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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/930,804	08/15/2001	Chris Haywood	06979.0012	3546
33356	7590	12/14/2004	EXAMINER	
SOCAL IP LAW GROUP 310 N. WESTLAKE BLVD. STE 120 WESTLAKE VILLAGE, CA 91362				NGUYEN, TOAN D
ART UNIT		PAPER NUMBER		
				2665

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	A HAYWOOD, CHRIS
	09/930,804		
	Examiner Toan D Nguyen	Art Unit 2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 15 August 2001.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-4 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-4 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 15 August 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date 3/24/03.

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bass et al (US 6,557,053) in view of Lee et al (US 6,442,674) further in view of Sun et al (US 6,574,194) and Manning (US 6,708,262).

For claim 1, Bass et al disclose queue manager for a buffer comprising:

a head FIFO memory (figure 1, reference 32) for sequentially delivering data packets

(col. 2 lines 10-12);

a tail FIFO memory (figure 1, reference 14) for storing an overflow of said data packets from said head memory (figure 1, reference 32), both said head and tail memories operating at a relatively high data rate equivalent to the rate of incoming data packet (col. 1 lines 14-15 and col. 2 lines 24-40);

a large capacity buffer memory (figure 1, reference 22) for temporarily storing data overflow from said tail memory whereby said FIFO memories in combination with said buffer memory for a variable size FIFO memory (col. 2 lines 24-41 and col. 4 lines 22-25).

Bass et al do not disclose a plurality of switching elements whereby some latency occurs between data packets and delivering data packets at a relatively slow rate. In an analogous art,

Sun et al disclose a plurality of switching elements whereby some latency occurs between data packets (col. 1 lines 37-40).

One skilled in the art would have recognized a plurality of switching elements whereby some latency occurs between data packets to use the teachings of Sun et al in the system of Bass et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use the plurality of switching elements whereby some latency occurs between data packets as taught by Sun et al in Bass et al's system with the motivation being to provide a switch system that has minimum latency but is low cost (col. 1 lines 44-45).

Bass et al in view of Sun et al do not disclose delivering data packets at a relatively slow rate. Lee et al disclose delivering data packets at a relatively slow rate (col. 2 lines 42-44).

One skilled in the art would have recognized delivering data packets at a relatively slow rate to use the teachings of Lee et al in the system of Bass et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use the delivering data packets at a relatively slow rate as taught by Lee et al in Bass et al's system with the motivation being governing a rate of uop arrival at the input line 110 of fill buffer 100 (col. 2 lines 45-47).

However, Bass et al in view of Lee et al do not disclose a large capacity buffer memory having an effectively lower clock rate than said FIFO memories. In an analogous art, Manning discloses disclose a large capacity buffer memory having an effectively lower clock rate than said FIFO memories (col. 1 lines 63-65).

One skilled in the art would have recognized a large capacity buffer memory having an effectively lower clock rate than said FIFO memories to use the teachings of Manning in the system of Bass et al. Therefore, it would have been obvious to one of ordinary skill in the art at

the time of the invention, to use the large capacity buffer memory having an effectively lower clock rate than said FIFO memories as taught by Manning in Bass et al's system with the motivation being provide a rate at which the DRAM may process commands is limited by the amount of time it takes to perform functions responsive to the commands (col. 1 lines 26-29).

For claim 2, Bass et al disclose where said head (figure 1, reference 32) and tail memories (figure 1, reference 14) have data blocks of a predetermined and same size, and said buffer memory has the same size data block whereby high efficiency data transfer between memories is obtained (col. 2 lines 24-36 and col. 3 lines 23-28).

For claim 3, Bass et al disclose where FIFO memories reside on a common semiconductor substrate and said buffer memory is remote (col. 1 lines 46-47).

For claim 4, Bass et al disclose wherein said buffer memory has a wider bus than said head and tail FIFO memories (figure 3, col. 3 lines 9-12 and col. 4 lines 9-10).

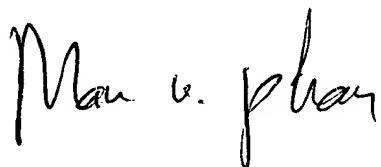
3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan D Nguyen whose telephone number is 703-305-0140. The examiner can normally be reached on Monday- Friday (7:00AM-4:30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Huy Vu can be reached on 703-308-6602. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2665

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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MAN U. PHAN
PRIMARY EXAMINER